Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently amended) ~~The system time of claim 1~~ A system timer for controlling the timing at which a communication device communicates, said system timer comprising:

a memory device adapted to store a set of software instructions:

a processor coupled to said memory device, said processor being adapted to execute any of said software instructions in any of a plurality of sequences, each of said sequences causing said processor to generate a corresponding set of control signals, each of said corresponding set of control signals being adapted to enable communication by said communication device in one of a multiplicity of communication formats, wherein each of said communication formats devices the timing at which a set of data is communicated by said communication device;

wherein said processor comprises a first processor and further wherein said communication device comprises a second processor, wherein said plurality of sequences in which said first processor executes said software instructions is controlled by said second processor.

3. (Original) The system timer of claim 2 wherein said system timer further comprises a memory register for storing addresses, said addresses indicating a set of locations at which at least some of said software instructions are stored in said memory device, wherein said first processor is adapted to extract said addresses from said memory register and to execute said software instructions located at said addresses thereby causing said first processor to execute said software instructions in a sequence defined by an order in which said addresses are stored in said memory register.

4. (Original) The system timer of claim 3 wherein said second processor controls said plurality of sequences in which said first processor executes said software instructions by controlling said order in which said addresses are stored in said memory register.

5. (Original) The system timer of claim 4 wherein said software instructions comprise a first software instruction that, when executed by said first processor, causes said first processor to extract one of said addresses stored in said memory register and to execute a second software instruction located at said one of said addresses provided that said second processor has caused at least one of said addresses to be stored in said memory register.

6. (Original) The system timer of claim 5 wherein said first software instruction further causes said first processor to execute a third software instruction stored in said memory device provided that said second processor has not stored said at least one address in said memory register, wherein an address at which said third software instruction is stored in said memory device is specified in said first software instruction.

7. (Original) The system timer of claim 2 wherein said set of software instructions stored in said memory device comprises a first instruction, said first instruction, when executed by said first processor, causing said first processor to execute a first sequence of software instructions provided that a condition has been satisfied by said second processor and further causing said first processor to execute a second sequence of software instructions provided that said condition has not been satisfied.

8. (Original) The system timer of claim 7 wherein said first sequence of software instructions begins with a second instruction located at an address specified in said first instruction.

9. (Original) The system timer of claim 7 wherein said condition comprises a mode bit being set to a first logic level.

10. (Original) The system timer of claim 7 wherein said condition comprises an equation being equal to a predefined value.

11. (Original) The system timer of claim 10 wherein said equation being equal to said predefined value depends upon whether a set of mode bits have been set by said second processor.

12. (Original) The system timer of claim 2 wherein said plurality of sequences comprises a first sequence that causes said communication device to perform single slot communication and wherein said second processor is adapted to modify said first sequence to a second sequence that causes said communication device to perform multi-slot communication.

13. (Original) The system timer of claim 2 wherein said second processor controls said sequence by setting a control bit stored in a memory register.

14. (Original) The system timer of claim 2 wherein said second processor comprises a digital signal processor.

15. (Original) The system timer of claim 2 wherein said second processor comprises a microprocessor.

16. (Currently amended) The system time of claim ~~1~~ 2 wherein said plurality of sequences comprises a first sequence of said software instructions that, when executed by said first processor, enables operation of said communication device in a first mode, wherein said plurality of sequences further comprises a second sequence of said software instructions that, when executed by said first processor, enables operation of said communication device in a second mode, and wherein said second processor is adapted to cause said first processor to switch between executing said first and second sequences thereby causing said communication device to switch between said first and second modes.

17. (Original) The system timer of claim 16 wherein said first mode comprises a stand by mode and wherein said second mode comprises an acquisition mode.

18. (Original) The system timer of claim 16 wherein said first mode comprises an acquisition mode and wherein said second mode comprises a steady state mode.

19. (Currently amended) The system timer of claim ~~1~~ 2 wherein said multiplicity of communication formats comprises a single slot communication format.

20. (Currently amended) The system time of claim ~~1~~ 2 wherein said multiplicity of communication formats comprises a multi-slot communication format.

21-36. (Cancelled)

37. (Original) A method for controlling the timing at which a communication device communicates, said communication device comprising a first processor and a system timer, said system timer comprising a second processor and a memory device adapted to store a set of software instructions, said method comprising the steps of:

causing said second processor to execute a set of software instructions in any of a plurality of sequences, each of said sequences causing said second processor to generate a corresponding set of control signals, each of said corresponding set of control signals being adapted to enable communication by said communication device in one of a multiplicity of communication formats, wherein each of said communication formats defines the timing at which a set of data is communicated by said communication device; and,

causing said first processor to define said sequences in which said second processor executes said software instructions.

38. (Original) The method of claim 37 wherein a first of said sequences causes said communication device to communicate in a first timing format and wherein a second of said sequences causes said communication device to communicate in a second timing format.

39. (Original) The method of claim 37 wherein said first timing format comprises a single slot timing format and wherein said second timing format comprises a multi-slot timing format.

40. (Original) The method of claim 37 wherein a first of said sequences defined by said first processor causes said communication device to operate in a first mode and wherein a second of said sequences defined by said first processor causes said communication device to communicate in a second mode.

41. (Original) The method of claim 39 wherein said first mode comprises a stand by mode and wherein said second mode comprises an acquisition mode.

42. (Original) The method of claim 40 wherein said first mode comprises an acquisition mode and wherein said second mode comprises a steady state mode.

43-52. (Cancelled)